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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,555	07/26/2001	Chih Hsin Wang	2102397-911400	8544

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,555	Applicant(s) WANG ET AL.
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Attorney's Docket Number: 2101397-911400

Filing Date: 7/26/2001

Claimed Priority Dates: 4/26/2001 (Provisional 60/287,047)
3/12/2001 (Provisional 60/275,517)
1/5/2001 (Provisional 60/242,096)
9/20/2000 (Provisional 60/234,314)

Applicant(s): Wang et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the election (paper no. 7) filed on 5/2/2002.

Election/Restrictions

1. Applicant's election without traverse of claims 27-36 in paper no. 7 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character **96** has been used to designate both a source (pp.12/ll.9) and a source line (pp.12/ll.10). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 27-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Line 3 of claim 27 recites the limitation "the substrate of a second conductivity type". There is insufficient antecedent basis for this limitation in the claim.

7. Lines 8-9 of claim 31 recite the limitation "the substrate having a second conductivity type". There is insufficient antecedent basis for this limitation in the claim.

8. Lines 11-12 of claim 31 recite the limitation "said substrate including over the channel regions". There is insufficient antecedent basis for this limitation in the claim.

9. Line 1 of claim 34 recites the limitation "each of the source regions". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Taketa (US 593979).

12. Taketa (fig. 6) shows all aspects of the instant invention including an electrically programmable and erasable memory device comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- first **3** and second **4** spaced-apart regions of a second conductivity type (n-type)
- a channel region **5** between the first **3** and second **4** spaced-apart regions
- a first insulation layer **6** disposed over the substrate **2**
- an electrically conductive floating gate **32** disposed over the first insulation layer **6** and extending over a portion of the channel region **5** and over a portion of the first region **3**
- an electrically conductive source region **14** disposed over and electrically connected to the first region **3** in the substrate **2**

wherein the source region has:

- a lower portion disposed adjacent to and insulated from the floating gate **32**
- an upper portion disposed over and insulated form the floating gate **32**

13. Regarding claim 28, Taketa (fig. 6) shows that the source-region upper-portion has a greater width than that of the source-region lower-portion.

14. Regarding claim 29, Taketa (fig. 6) shows the source region **14** having a substantially T-shaped cross-section.

15. Regarding claim 30, Taketa (fig. 6) shows the memory device further comprising:

- a second insulation layer **8** disposed over and adjacent to the floating gate **32** and a having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col.9/ll.37)
- an electrically conductive control gate **9** having:
  - a first portion adjacent to the second insulation layer **8** and floating gate **32**
  - a second portion over a portion of the second insulation layer **8** and a portion of the floating gate **32**

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 31-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Taketa in view of Kao (US 6211547).

19. Taketa (fig. 6) shows most aspects of the instant invention including an array of electrically programmable and erasable memory devices comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- a plurality of active regions (see, *e.g.*, the cross-sectional view shown in fig. 6 and the circuit diagram shown in fig. 11) , each of the active regions including a column of pairs **31a 31b** of memory cells extending in a first direction, each of the memory cell pairs **31a 31b** including:
  - a first region **3** and a pair of second regions **4** spaced apart and of a second conductivity type (n-type)
  - channel regions **5** between the first region **3** and the second regions **4**
  - a first insulation layer **6** disposed over the substrate **2** and over the channel regions **5**
  - a pair of electrically conductive floating gates **32** disposed over the first insulation layer **6** and extending over a portion of the channel region **5** and over a portion of the first region **3**
  - an electrically conductive source region **14** disposed over and electrically connected to the first region **3** in the substrate **2**

wherein the source region **14** has:

- a lower portion disposed adjacent to and insulated from the floating gate **32**
- an upper portion disposed over and insulated form the floating gate **32**

However, the cross-sectional views of the memory-cell array in Taketa's drawings (see, *e.g.*, fig. 6) fail to show spaced-apart isolation regions parallel to one another in the first direction such that an active region is between each pair of adjacent isolation regions. Nonetheless, the skilled artisan will understand that a cross-sectional view across Taketa's drawing will show such isolation regions. See, for example, Kao (figs. 1-3), who shows a conventional memory-cell array similar to Taketa's. A top view (fig. 3) of Kao's conventional structure shows spaced apart isolation regions (FOX) parallel to one another in a first direction such that an active region is between each pair of adjacent isolation regions. Moreover, Kao teaches (col.3/ll.11-15) that it is conventionally known that isolation regions are used to separate adjacent columns of memory-cell transistors.

Accordingly, it would have been obvious to one of ordinary skill in the art that Taketa's memory device includes spaced apart isolation regions parallel to one another in the first direction such that an active region is between each pair of adjacent isolation regions, as taught by Kao, since it is conventionally known that isolation regions are used to separated adjacent columns of memory-cell transistors, i.e., active regions.

20. Regarding claim 32, Taketa (fig. 6) shows that the source-region upper-portion has a greater width than that of the source-region lower-portion.

21. Regarding claim 33, Taketa (fig. 6) shows the source region **14** having a substantially T-shaped cross-section.

22. Regarding claim 34, Taketa (fig. 11) shows the source region **14** of each of the memory-cell pairs **31a 31b** extending in a second direction substantially perpendicular

to the first direction such that it intercepts one of the memory cell pairs **31a 31b** in each of the active regions. Kao (fig. 3) shows the isolation regions (FOX) parallel to the first direction.

23. Regarding claim 35, Taketa (fig. 6) shows the memory device further comprising:

- a second insulation layer **8** disposed over and adjacent to each of the floating gate **32** and a having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col.9/ll.37)
- a pair of electrically conductive control gates **9**, each control gate having:
  - a first portion adjacent to the second insulation layer **8** and one of the floating gates **32**
  - a second portion over a portion of the second insulation layer **8** and a portion of one of the floating gates **32**

24. Regarding claim 36, Taketa (fig. 11) shows each of the control gates **9** extending across the active regions in a second direction substantially perpendicular to the first direction and intercepting one of the memory-cell pairs **31a 31b** in each of the active regions. Kao (fig. 3) shows the isolation regions parallel to the first direction.

Conclusion

25. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989) The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724** The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 8.00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Marcos Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

27. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

28. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314-326	7/17/2002
Other Documentation: PLUS Analysis	7/17/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	7/17/2002

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July 17, 2002

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